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University of Cyprus

School of Engineering
Department of Electrical and Computer Engineering

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Department of Electrical and Computer Engineering

Title: *"NeuroChiplets: Energy efficient IP blocks for embedded A.I. and machine learning"*

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Abstract:

The NeuroChiplets project in my lab is aimed at the design of energy efficient cognitive processing accelerators for embedded A.I and machine learning at the "edge". IoT devices are often thought as the "edge" of a large sophisticated cloud processing infrastructure. Autonomous operation and decision making coupled with real-time ability to do local-processing before transmitting the data/information necessitates feature-driven "intelligent" sensing nodes with extreme energy efficiency. In this talk I will outline the design methodology for energy efficient neuromorphic accelerators aimed at IoT devices that combine Ultra-Low-Voltage (ULV) circuit techniques with brain-inspired chip-multiprocessing. More specifically, I will discuss in detail four of a dozen IP core/accelerators for (i) probabilistic speech, sound and language processing (ii) mixed signal vector matrix processing for sparse and dense linear algebra (iii) morphological processing for embedded vision (iv) analog convolutional networks for recognition in standard flash technology (SST ESF3 SuperFlash cells). Our IP is developed in the cost-effective Global Foundries 65/55 nm technology node with custom designed I/O pads and CMOS libraries capable of operating between 0.4 and 1.2 Volts, allowing for dynamic voltage scaling. Measured performance for sub-systems performing fixed point 8-12 bit operations yields ~10 TOPS/W while for binary processing it exceeds 100 TOPS/W. The IP blocks are designed with a common interface to an energy efficient crossbar switched circuit network on chip (NOC) that connects to an ARM M0 supervisory processor and an M3 general purpose processor through standard AMBA bus.

Biography:

Andreas G. Andreou is a professor of electrical and computer engineering, computer science and the Whitaker Biomedical Engineering Institute, at Johns Hopkins University. Andreou is the co-founder of the Johns Hopkins University Center for Language and Speech Processing. Research in the Andreou lab is aimed at brain inspired microsystems for sensory information and human language processing. Notable microsystems achievements over the last 25 years, include a contrast sensitive silicon retina, the first CMOS polarization sensitive imager, silicon rods in standard foundry CMOS for single photon detection, hybrid silicon/silicone chip-scale incubator, and a large scale mixed analog/digital associative processor for character recognition. Significant algorithmic research contributions for speech recognition include the vocal tract normalization technique and heteroscedastic linear discriminant analysis, a derivation and generalization of Fisher discriminants in the maximum likelihood framework. In 1996 Andreou was elected as an IEEE Fellow, "for his contribution in energy efficient sensory Microsystems."