Πανεπιστήμιο Κύπρου
University of Cyprus

**School of Engineering
Department of Electrical and
Computer Engineering**

IEEE
Advancing Technology
for Humanity

Department of Electrical and Computer Engineering

Title: « Ultra Low Power Design of Smart Wireless Body Sensor Nodes»

**Prof. David Atienza Alonso, Director, Embedded Systems Laboratory, EPFL,
Switzerland**

Wednesday, 15th January 2014, 16:30 – 17:30
**Room ΧΩΔ 02 – 016, New Campus
University of Cyprus**

Abstract:

Latest progress in microelectronics have enabled the miniaturization of processing elements, radio transceivers and sensing elements of a large array of physiological phenomena. This situation has made plausible to realize low cost, low power, miniaturized, yet, smart sensor nodes needed to develop wireless body-area sensor networks (WBSN). However, the inherent resource-constrained nature of these systems, coupled with the harsh operating conditions and stringent autonomy requirements, pose important design challenges to make them provide automated analysis for complex biological signals. This presentation addresses system-level design of next-generation smart WBSN platforms for personal health monitoring systems, and highlights the unsustainable energy cost incurred by the relatively straightforward wireless streaming of raw sensor data. To achieve the extended autonomy required by long-term ambulatory monitoring, this talk advocates for enabling more embedded intelligence onboard these sensor nodes through a new system-level design approach. This approach exploits the bio-signals features to apply the new compressive sensing paradigm in the design of specialized near-threshold computing and memory blocks in order to deploy ultra-low power (ULP) multi-core processing architectures for automated bio-signals analysis on WBSN. To illustrate the effectiveness of this approach, this talk focuses on electrocardiogram (ECG) monitoring applications and show how it is possible to achieve portable ULP ECG arrhythmia detection systems that can operate autonomously for long periods of time and support a graceful quality degradation of the system output based on the available power.

Biography:

David Atienza is professor of EE and director of the Embedded Systems Laboratory (ESL) at EPFL, Switzerland. He received his MSc and PhD degrees in computer science and engineering from UCM, Spain, and IMEC, Belgium, in 2001 and 2005, respectively. His research interests focus on system-level design methodologies for high-performance multi-processor Systems-on-Chip (MPSoC) and low-power embedded systems, including new thermal-aware design for 2D and 3D MPSoCs, design methods and architectures for wireless body sensor networks, dynamic memory management and interconnection hierarchy optimizations. In these fields, he is co-author of more than 200 publications in prestigious journals and international conferences, several book chapters and six U.S. patents. He received the IEEE CEDA Early Career Award in 2013, the ACM SIGDA Outstanding New Faculty Award in 2012 and a Faculty Award from Sun Labs at Oracle in 2011. He is a Distinguished Lecturer (2014-2015) of the IEEE CASS. He has also earned two best paper

awards at the VLSI-SoC 2009 and CST-HPCS 2012 conference, and five best paper award nominations at the DAC 2013, DATE 2013, WEHA-HPCS 2010, ICCAD 2006 and DAC 2004 conferences. He serves or has served as associate editor of IEEE Trans. on Computers (TC), IEEE Design & Test of Computers (D&T), IEEE Trans. on CAD (T-CAD), and Elsevier Integration. He is an elected member of the Executive Committee of the IEEE CEDA since 2008, and was GOLD member of the Board of Governors of IEEE CASS from 2010 to 2012. He is Senior Member of IEEE and ACM.ACM.