All You Will Never Have Wanted to Know on Branch Predictors

Dr. André Seznec
IRISA/INRIA Rennes, France

Thursday, April 5, 2012 / 17:00-18:00

Room 148, Building 12 Faculty of Pure and Applied Sciences,

New Campus

Abstract: Dynamic branch prediction is still one of the most important processor performance enabler. Branch prediction was introduced by J. Smith around 1980, then using branch history was proposed in 1991. Then, for about ten years, branch prediction was a hot research topic. Since 2000, interest of the computer architecture research community for branch prediction has faded. However, at the same time, there has been more progress on branch prediction accuracy between 2002 (presentation of the EV8 branch predictor) and 2006 (2nd Championship Branch Prediction) than during the 10 previous years.
In this talk, I will introduce the geometric history length predictors, O-GEHL and TAGE. I respectively presented O-GEHL at the 1st Championship on Branch Prediction (CBP-1) in december 2004 and TAGE at the 2nd Championship on Branch Prediction (CBP-2) in december 2006. Both O-GEHL and TAGE combine several prediction tables. They use a geometric series of history lengths for indexing these prediction tables. O-GEHL computes its final prediction through an adder tree, while TAGE relies on partial-tag match. TAGE constitutes currently the state-of-the-art in branch prediction as confirmed by the 3rd Championship on Branch Prediction (june 2011).

Biography
André Seznec got a Doctorat ès Sciences in computer sciences from University of Rennes~I in June 1987. He was hired as a researcher at INRIA Rennes in October 1986. He was promoted as Research Director at INRIA in 1994 and as Senior Research Director (DR1) in 2002. He has been leading the CAPS then ALF project-team at INRIA Rennes since 1994. From Feb. 1999 to Feb. 2000, he spent a sabbatical yearwith the VSSAD, Alpha Development Group at Compaq (Shrewsbury, Massachusetts). André Seznec has focused his research on processor architecture since the beginning of his Ph.D. thesis in 1983. He has made many contributions on vector supercomputers, pipeline architecture and SMT and multicore architecture. His most significant contributions are on cache architecture and branch prediction. André Seznec has published more than 20 papers in international journals including IEEE transactions on computers, IEEE transaction on parallel and distributed computing, ACM Transactions on Architecture and Code Optimizations, Journal on Instruction Level Parallelism and ACM Transaction on Modeling and Computer Simulations. He has published over 40 papers in international conferences on computer architecture. André Seznec has directed 15 Ph. D. thesis. In 2010, André Seznec has got an ERC advanced grant.