Πανεπιστήμιο Κύπρου
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School of Engineering
Department of Electrical and Computer Engineering

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Department of Electrical and Computer Engineering

Title: "**Parallelization of test pattern generation in multi-core systems**"

Stavros Hadjitheophanous
Ph.D candidate at Department of Electrical and Computer Engineering, University of Cyprus.

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Room ΠΤΕΡ Ε116, Old Campus

Abstract:

Moving into the multi-core era has multiplied the processing power of computing systems. Nevertheless, this capability is not fully utilized when parallelism is not invoked by software. EDA processes can exhibit high level of parallelism, yet parallelization is not straight forward and can certainly affect the quality of the obtained result. In this talk we will present some fundamental concepts of VLSI testing process and discuss the effect of parallelization on a dynamic compaction-based ATPG method. The parallelization process is initialized by a hybrid fault partitioning technique that favors load balancing among available processing units. Test generation is then carried out in a distributed fashion, taking advantage of the system's shared memory architecture. In the presented work we investigate two scenarios within the same load balancing approach. One applies a final composition step of the individual results obtained by all processing units in an attempt to further reduce the test set size at the expense of extra time. The other one skips this step with the goal of maximizing the overall speedup, in a similar manner that most current parallel methods do. The obtained results demonstrate that a final composition step is very effective in reducing the test set size while maintaining very good speedup, as the number of utilized cores increases.

Biography:

Stavros Hadjitheophanous received his Bachelor's Degree in Computer Engineering from the University of Cyprus in 2009. In 2010 Stavros received his MSc degree from University of Bristol in the subject Advance Computing Internet Technologies with Security. Currently he is a Ph.D. candidate in the Department of Electrical and Computer Engineering at the University of Cyprus. He is also working as a Researcher at the KIOS Research Center for Intelligent Systems and Networks. His research interests include design and CAD algorithms for automatic testing for VLSI, multi-core algorithms for high quality testing, network security and machine vision applications.